<u>REMARKS</u>

The Examiner is thanked for the indication that claims 4-6 are allowed.

Claims 1-3 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Honda et al. (U.S. Publication No. 2002/0030672) (hereinafter "Honda"). This rejection is respectfully traversed for at least the following reasons, in addition to the technical distinctions between claims 1-3 of the instant application and Honda as explained in previously-filed responses in this application.

Applicants respectfully submit that independent claim 1 of the instant application includes particular distinctions from the disclosure of <u>Honda</u> and as a result, independent claim 1 has not been newly-amended in the instant response. After careful study, Applicants believe that the Office Action's rejection is based on a technical misunderstanding of the disclosure of <u>Honda</u> for at least the following reasons.

Applicants respectfully submit that the 1H line luminance distribution analyzing circuit 3 of Honda does not create the accumulated frequency data for each field in the manner specifically described in independent claim 1 of the instant application. Applicants respectfully submit that this is clear from the teachings in paragraphs 0036 to 0038 of Honda. More particularly, paragraph 0036 discloses that the memory 300 of the circuit 3 has 256 storage locations DF₀ to DF₂₅₅ (see Fig. 3 of Honda), and each of these storage locations has an initial value "zero." Applicants respectfully submit that the storage location DF₀ is a location to store the frequency of the darkest level. Also, the storage location DF₁ is a location to store the frequency of the second darkest level. The storage location DF₂₅₅ is a location to store the frequency of the brightest level.

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Applicants respectfully submit that paragraph 0037 of Honda discloses that, for example,

the circuit 301 of the circuit 3 increments frequency data DF₁ by one, each time it is supplied

with one pixel data D having the second darkest level. One display line has m pixel data because

there are m column electrodes (see Fig. 1 of Honda). Thus, Applicants respectfully submit that

the circuit 301 repeats the incrementing operation m times. Upon each incrementing operation,

"1" is added to one of the data DF₁ to DF₂₅₅. These data DF₁ to DF₂₅₅ are stored in the memory

300. When the incrementing operation is done for one display line (or m times), the circuit 301

retrieves the data DF₀ to DF₂₅₅ from the memory 300 and supplies them to the circuit 302. The

data DF₀ indicates how many times pixel data having the darkest level is supplied in a single

display line. The data DF₁ indicates how many times pixel data having the second darkest level

is supplied in the single display line. The data DF₂₅₅ indicates how many times pixel data having

the brightest level is supplied in the single display line.

Applicants respectfully submit that paragraph 0038 of Honda then mentions that the

circuit 3 (or the circuit 302 in the circuit 3) accumulates the frequency data DF₀ to DF₂₅₅ by the

following calculation:

 $AC_0 = DF_0$

 $AC_1 = DF_0 + DF_1$

 $AC_2 = DF_0 + DF_1 + DF_2$

.

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• • • • •

 $AC_{255} = DF_0 + DF_1 + DF_2 + ... + DF_{254} + DF_{255}$

Therefore, Applicants respectfully submit that the resulting accumulated data AC₁ to

AC₂₅₅ are still the accumulated data for each display line, not for each field.

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Paragraph 0039 of <u>Honda</u> discloses that the maximum value of each accumulated data AC is m because each display line has m pixel data (or m pixels). If the data is accumulated for each field, the maximum value of accumulated data AC should be m x n because each field has m x n pixels.

Paragraphs 0040 and 0042-0045 also deal with a story of each display line, not for each field.

As a result, for at least the foregoing reasons, Applicants respectfully submit that Honda does not anticipate independent claim 1 of the instant application. In particular, the features associated with the brightness frequency data circuit, as particularly described in independent claim 1 of the instant application is not disclosed by Honda.

Accordingly, Applicants respectfully assert that the rejections under 35 U.S.C. § 102(b) should be withdrawn because <u>Honda</u> does not teach or suggest each feature of independent claim 1 of the instant application. As pointed out in MPEP § 2131, "[t]o anticipate a claim, the reference must teach every element of the claim." Thus, "[a] claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. Verdegaal Bros. v. Union Oil Co. Of California, 2 USPQ 2d 1051, 1053 (Fed. Cir. 1987)."

Furthermore, Applicants respectfully assert that dependent claims 2-3 are allowable at least because of their dependence from claim 1, and the reasons set forth above. The remaining claims 4-6 have been indicated as allowed by the Examiner.

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CONCLUSION

In view of the foregoing, Applicants submits that the pending claims are in condition for allowance, and respectfully request reconsideration and timely allowance of the pending claims. Should the Examiner feel that there are any issues outstanding after consideration of this response, the Examiner is invited to contact Applicants' undersigned representative to expedite prosecution. A favorable action is awaited.

EXCEPT for issue fees payable under 37 C.F.R. § 1.18, the Commissioner is hereby authorized by this paper to charge any additional fees during the entire pendency of this application including fees due under 37 C.F.R. § 1.16 and 1.17 which may be required, including any required extension of time fees, or credit any overpayment to Deposit Account No. 50-0573. This paragraph is intended to be a **CONSTRUCTIVE PETITION FOR EXTENSION OF TIME** in accordance with 37 C.F.R. § 1.136(a)(3).

Respectfully submitted,

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Dated: October 1, 2008

By:

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